Conference Day 1
Monday, August 20

HOT CHIPS 19

9:00 - 9:15am	**Opening Remarks**		
9:15 - 10:45	**Session One**	**IBM POWER6™**	
	Fault-Tolerant Design of the IBM POWER6™ Microprocessor		IBM
	System Performance Scaling of IBM POWER6™ Based Servers		IBM
	The Third Generation of IBM's Elastic Interface on POWER6™		IBM
11:15 - 12:15	**Keynote**	**Digital Gaia**	
	Vernor Vinge	Computer Scientist, Science Fiction Writer, author of *True Names* and *Rainbows End*	
12:15 - 1:15	**Lunch**		
1:15 - 2:45	**Session Two**	**Multi-Core and Parallelism I**	
	NVIDIA GeForce 8800™ GPU		NVIDIA
	The NVIDIA GPU Parallel Computing Architecture & CUDA Programming Model		NVIDIA
	Performance Insights of Executing Non-Graphics Applications on the NVIDIA GeForce 8800™ & the CUDA™ Parallel Programming Environment		NVIDIA, UIUC
3:15 - 5:15	**Session Three**	**Multi-Core and Parallelism II**	
	AMD's Radeon™ HD 2900 - 2nd Generation Unified Shader Architecture		AMD
	Teraflops Prototype Processor with 80 Cores		Intel
	TRIPS: A Distributed Explicit Data Graph Execution (EDGE) Microprocessor		UT - Austin
	The Tile Processor™ Architecture: Embedded Multicore for Networking and Digital Multimedia		Tilera
5:45 - 7:15	**Session Four**	**Embedded and Video**	
	SH-X3: Flexible SuperH Multi-Core for High-Performance and Low-Power Embedded System		Renasas, Hitachi
	An Innovative HD Video and Digital Image Processor for Low-Cost Digital Entertainment Products		Texas Instruments
	Professional H.264/AVC CODEC Chip-Set for High-Quality HDTV Broadcast Infrastructure and High-End Flexible CODEC Systems		NTT Cyber Space Labs
7:15 - 8:15	**Dinner**		
8:15 - 9:45	**Panel Discusson**	**What's next beyond CMOS?**	
	Moderator:	Norm Jouppi	HP Labs
	Panelists:	Mark Horowitz	Stanford University,
		John Kubiatowicz	UC Berkeley,
		Mike Mayberry	Intel,
		Ghavam Shahidi	IBM,
		Stan Williams	Hewlett-Packard

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Conference Day 2
Tuesday, August 21

8:00-9:30	**Session Five**	**Technology and Software Directions**	
	Multiterabit Switch Fabrics Enabled by Proximity Communication		Sun Microsystems Labs
	Thyristor RAM (T-RAM) - A High-Speed High-Density Embedded Memory Technology for Nano-Scale CMOS		T-RAM Semiconductor
	Raksha: A Flexible Architecture for Software Security		Stanford University
9:30-10:30	**Session Six**	**Wireless**	
	A 2x2 MIMO Baseband for High-Throughput Wireless Local-Area Networking (802.11n)		Broadcom
	A 4 Gbps Wireless True Uncompressed 1080p-Capable HD A/V Transceiver using 60 GHz		SiBeam
10:30-11:00			
11:00-12:00	**Keynote**		
	Multicore and Beyond: Evolving the x86 Architecture		
	Phil Hester, Chief Technology Officer, AMD		
12:00 - 1:00	**Lunch**		
1:00 - 1:30	**Special Presentation**		
	Wireless Broadband and Entrepreneurship in America		
	Reed Hundt, Vice-Chairman, Frontline Wireless, Former Chair, FCC		
1:30-3:00	**Session Seven**	**Networking**	
	Chesapeake: A 50 Gbps Network Processor and Traffic Manager		Bay Microsystems
	Tolapai - A System on a Chip with Integrated Accelerators		Intel
	Fulcrum's FocalPoint II - A 300ns, 240Gb/s Switch/Router		Fulcrum Microsystems
3:20-4:50	**Session Eight**	**Mobile PC Processors and Chipsets**	
	Advanced Power Management Features in Penryn: 45nm Next Generation Intel Core™ 2 Duo		Intel
			Fulcrum Microsystems
	Next Generation Mobile X86 Processor from AMD		AMD
	nForce 680i and 680a, NVIDIA's Next Generation Platform		NVIDIA
4:50-5:10			
5:10-6:10	**Session Nine**	**Big Iron**	
	VictoriaFalls - Scaling Highly-Threaded Processor Cores		Sun Microsystems
	The Next Generation Mainframe Microprocessor		IBM
6:10-6:15	**Closing Remarks**		